Indian Institute of Technology Patna

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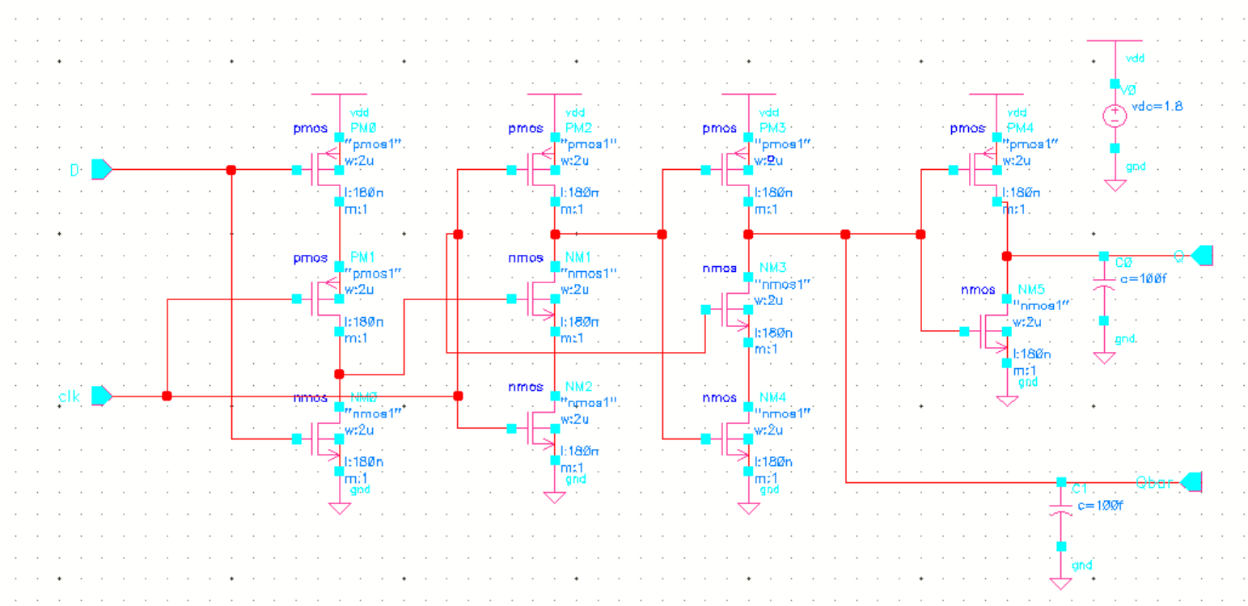
**Roll No. –** 2411EE23

**Project** – Classical PLL

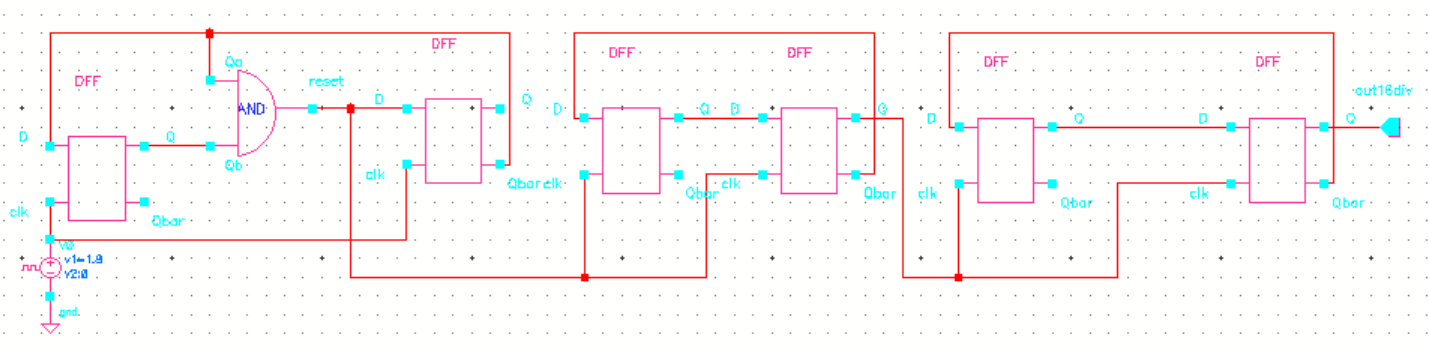
**Divider\_48**

**Circuit Diagrams:**

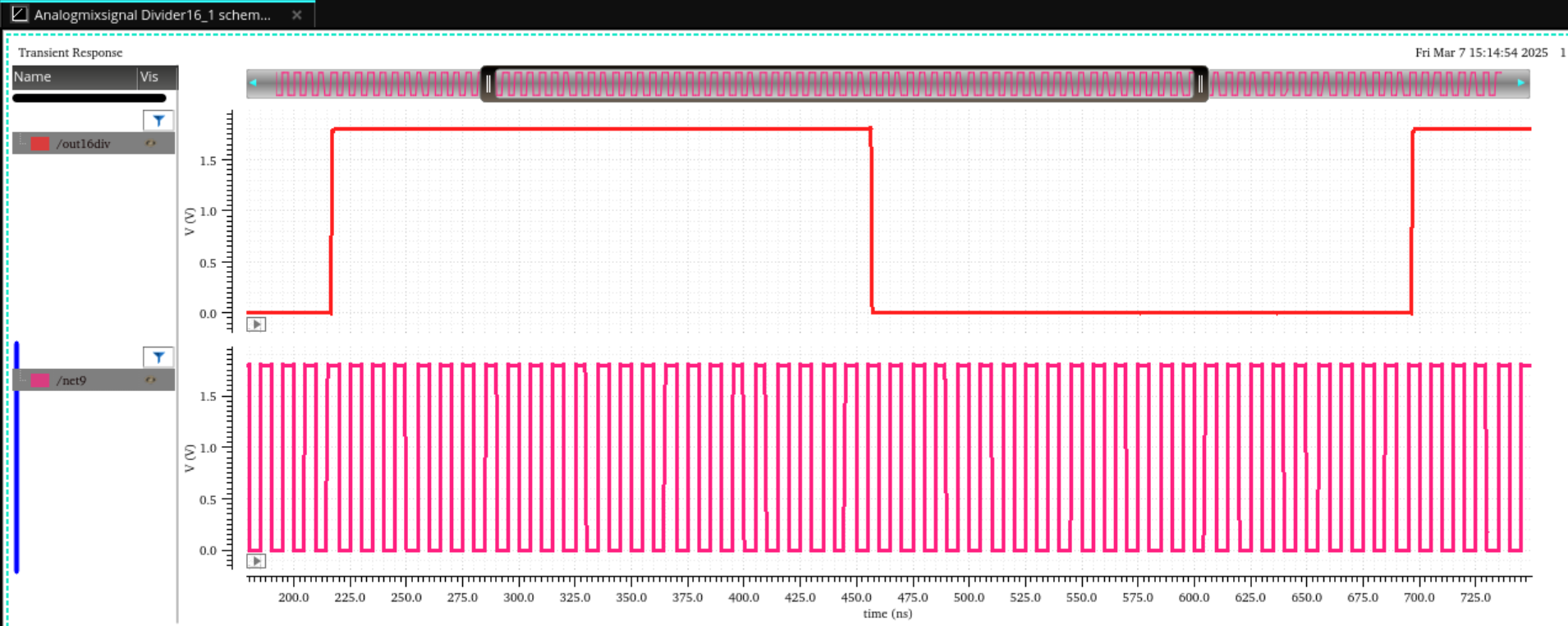
1. Using D-Flip Flops, we make divide by 48 circuit, it consist of a divide by 3 and divide by 16.



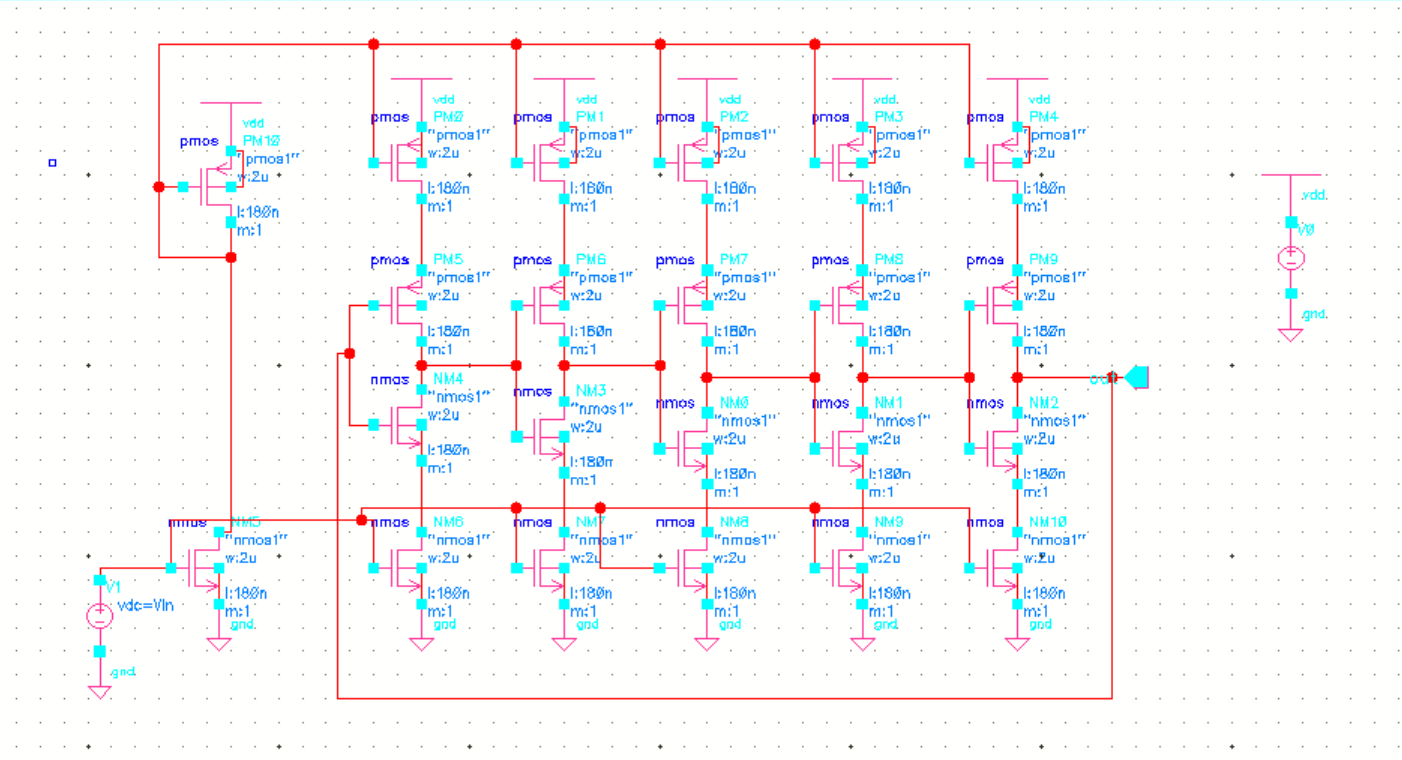
**Fig 1:** A D-Flip Flop



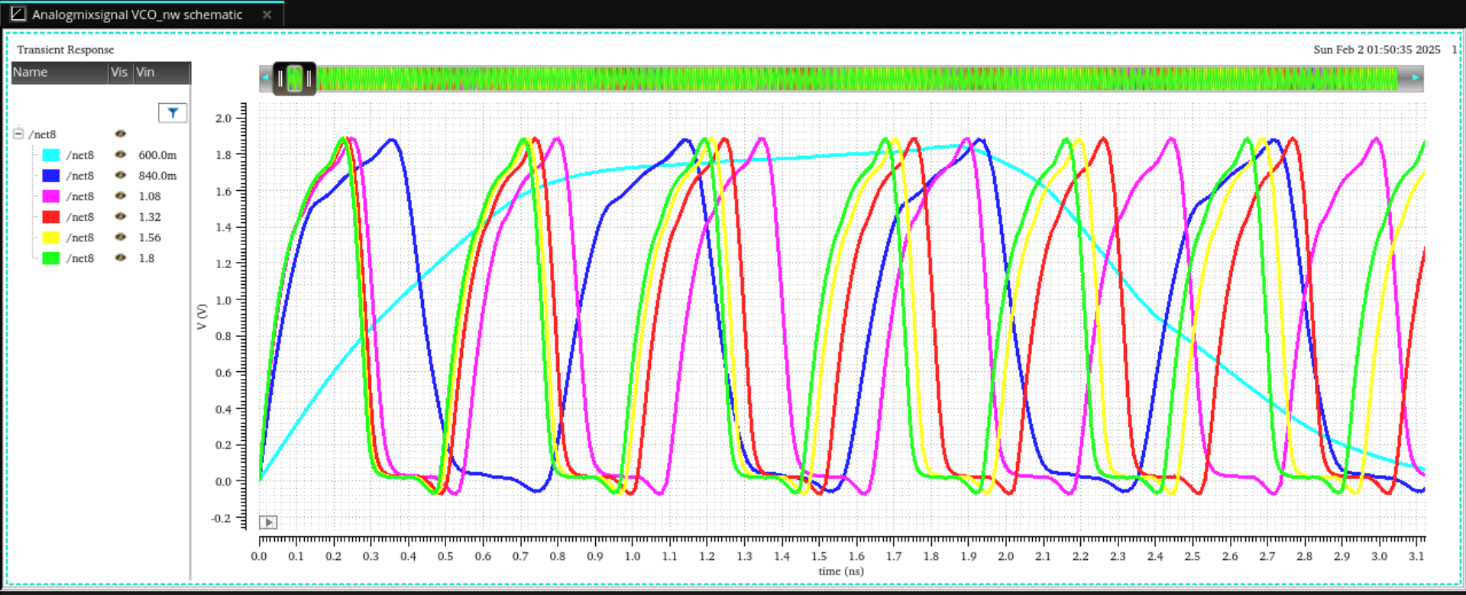
**Fig 2:** Divide by 48 circuit

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**Fig 3:** Output waveform of divide by 48 circuit

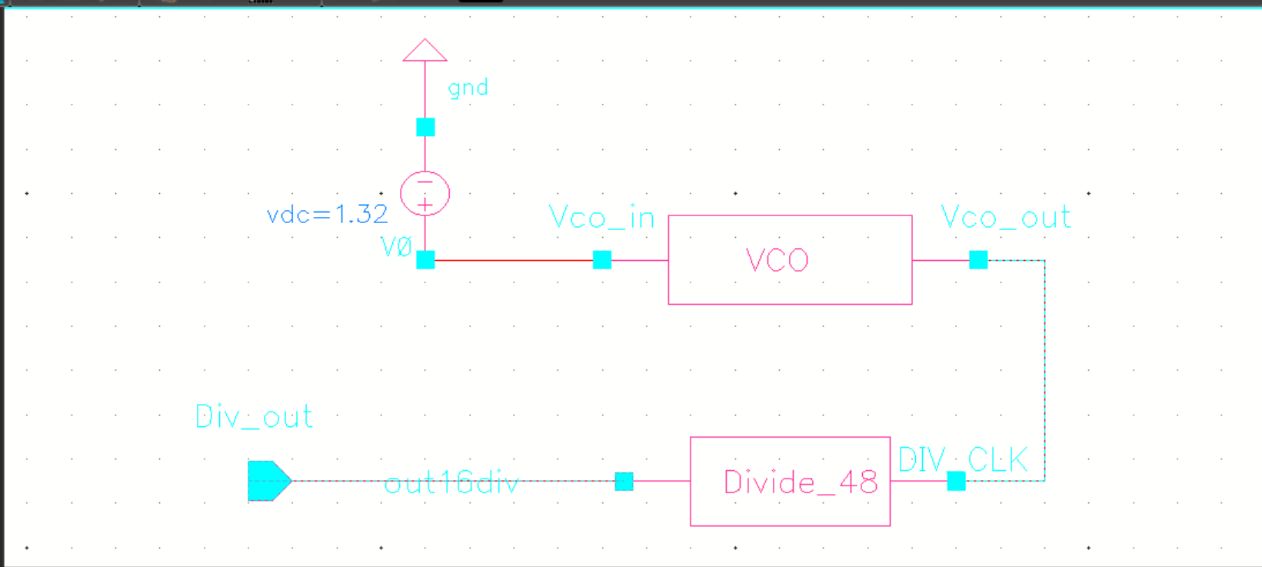


**Fig 4:** Circuit Diagram of current Starved VCO



**Fig 5** : Output waveform of VCO using Parametric analysis

1. **Integration of the above designed Divide by 48 circuit with VCO**



**Fig 6:** Circuit of integration of VCO and Divider



**Fig 7**: Output waveform of Divider and VCO

**Calculation**

Since, f=1/T

For VCO,

t2 - t1 = (19.3177- 18.259)ns = 1.0587ns

So, f = (1/ 1.0587)GHz = 944.55 MHz

For Divider,

t2 - t1 = (62.6303 - 18.0665) ns = 44.5638 ns

So, f = (1/44.5638)GHz = 22.44 MHz

Since M = (f vco/f div) = 944.55/22.44 = approx. 48